

## IN THE CLAIMS

Please amend the claims to the following:

1. (Currently Amended) A method comprising:

receiving from a processor a plurality of write transactions, which are identified by write combined in a the processor as write combinable write transactions;

storing data associated with the plurality of write transactions in a buffer of an input/output (I/O) hub to form write combined data in response to the plurality of transaction being identified as write combinable write transactions; and

flushing the write combined data associated with the plurality of write transactions to an I/O device according to a protocol between the I/O hub and the processor.
2. (Original) The method of claim 1, wherein flushing the data to the I/O device includes:

determining whether a flush signal has been received from the processor; and

flushing the data if the flush signal has been received, the protocol including an signaling protocol.
3. (Currently Amended) The method of claim 2, further including sending a write completion signal to the processor for each of the plurality of write transactions before the data is flushed to the I/O device, each write completion signal verifying buffering of a corresponding write transaction.
4. (Original) The method of claim 3, further including sending a flush completion signal to the processor after the data is flushed to the I/O device.

5. (Original) The method of claim 2, wherein flushing the data if the flush signal has been received further includes:

tagging the buffer with a first source identifier associated with one or more of the write transactions;

detecting a second source identifier associated with the flushing signal;

comparing the second source identifier to the first source identifier; and

flushing the data to the I/O device if the second source identifier matches the first source identifier.

6. (Original) The method of claim 5, further including repeating the comparing for a plurality of buffers, each buffer corresponding to an I/O port.

7. (Original) The method of claim 1, wherein flushing the data to the I/O device includes:

determining whether a latency condition exists; and

flushing the data if the latency condition exists, the protocol including a timing protocol.

8. (Original) The method of claim 7, further including sending a write completion signal to the processor for each of the write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction.

9. (Original) The method of claim 7, wherein the latency condition includes a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state.

10. (Original) The method of claim 1, wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device.

11. (Original) The method of claim 1, wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

12. (Currently Amended) An input/output (I/O) hub comprising:

receiving logic to receive a first write transaction and a second write transaction from a processor, the first and the second write transactions to reference partial data, wherein the processor is to identify the first and the second partial write transactions as write combinable write combined in a processor,

storage logic coupled to the receiving logic to store the partial data associated with referenced by the first and second write transactions as write combined data in response to the first and second write transactions being identified as write combinable; and

flushing logic coupled to the storage logic to flush the write combined data to an I/O device in response to a protocol event.

13. (Previously Amended) The I/O hub of claim 12, wherein the protocol event includes special flush signal to be received by the receiving logic from the processor.

14. (Currently Amended) The I/O hub of claim 13, further comprising transmission logic to send a first and a second write completion signal to the processor for the first and the second write transactions, respectively, before the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify successful storage of the partial data associated with referenced by the first and the second write transactions, respectively.

15. (Previously Amended) The I/O hub of claim 14, wherein the transmission logic is also to send a flush completion signal to the processor after the write combined data is flushed to the I/O device.

16. (Previously Amended) The I/O hub of claim 12, further comprising write combining logic to determine whether a latency condition exists, wherein the protocol event includes the latency condition.

17. (Previously Amended) The I/O hub of claim 16, further comprising transmission logic to send a first and a second write completion signal to the processor for the first and the second write transactions, respectively, as the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify flushing of the first and the second write transactions, respectively.

18. (Previously Amended) The I/O hub of claim 16, wherein the latency condition includes a delay in receiving a next third combinable write transaction from the processor and an interface to the I/O device being in an idle state.

19. (Currently Amended) The I/O hub of claim 12, wherein the storage logic includes a plurality of buffers, each buffer corresponding to an I/O port, and wherein the flushing logic is to flush data from one of the plurality of buffers corresponding to the processor in response to a protocol event associated with the processor.

20. (Previously Amended) The I/O hub of claim 12, wherein the write combined data is to be longer than one cache line.

21. (Currently Amended) A system comprising:

an input/output (I/O) device;

~~a peripheral components interconnect (PCI) express bus coupled to the I/O device;~~

a processor to identify a plurality of write transactions as write combinable and to transmit  
the plurality of write transactions, wherein each of the write transactions are to be  
associated with partial data; and

~~a chipset having an I/O hub coupled to the I/O device the PCI express bus and the processor,~~  
the I/O hub having ~~a buffer~~ and a write combining module to receive ~~the~~ a plurality  
of write transactions ~~to be write combined~~ from the processor, to store ~~the~~ partial  
data associated with the plurality of write transactions ~~in the buffer~~ to form a write  
combined data set in response to the plurality of write transactions being identified  
as write combinable, and to flush the write combined data set to the I/O device in  
response to a protocol event associated with the processor, the write combined data  
set to be longer than one cache line.

22. (Previously Amended) The system of claim 21, wherein the protocol event includes a flush signal from the processor.

23. (Currently Amended) The system of claim 22, wherein the processor is to generate the flush signal in response to if a flushing event ~~has occurung[[ed]]~~ and a write combine history indicating[[es]] that one or more combinable write transactions have been issued by the processor.

24. (Original) The system of claim 23, wherein the write combine history is to track combinable write transactions for a particular processor thread.

25. (Original) The system of claim 24, wherein the write combine history is to further track combinable write transactions for a particular I/O hub.

26. (Currently Amended) The system of claim 22, wherein the I/O hub is included in a the chipset that includes a plurality of I/O hubs, the processor to send the flush signal to each of the plurality of I/O hubs.

27. (Previously Amended) The system of claim 26, wherein the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the flush signal.

28. (Previously Amended) The system of claim 21, wherein the protocol event includes a latency condition.

29. (Original) The system of claim 21, wherein the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute associated with the write transactions.

30. (Original) The system of claim 21, further including a point-to-point network interconnect coupled to the processor and the I/O hub, the network interconnect having a layered communication protocol.

31. (Currently Amended) A method comprising:

receiving a plurality of write transactions from a processor, the plurality of write transactions being identified as write combinable transactions and being destined for an input/output (I/O) device;

storing data associated with the plurality of write transactions to a buffer of the I/O hub in response to the plurality of write transactions being identified as write combinable transactions;

determining whether a latency condition exists, the latency condition including a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state;

flushing the data to the I/O device if the latency condition exists; and

sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction.

32. (Original) The method of claim 31, wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device.

33. (Original) The method of claim 31, wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

34. (Currently Amended) A processor comprising:
- page table logic to identify a page in a memory; wherein the page table logic is to associate
- a write combining attribute to indicate that partial writes from the page are
- combinable;
- write combining logic to combine a plurality of partial writes from the page into a combined
- write in response to the write combining attribute associated with the write
- combining attribute to indicate that partial writes from the page are combinable; and
- transmit logic to transmit the combined write to an external device.
- A machine readable medium to store a set of instructions that direct a computer to function in a
- specified manner when executed, the instructions comprising:
- receiving a plurality of write transactions to be write combined from a processor;
- storing data associated with the plurality of write transactions to in a buffer of an
- input/output (I/O) hub to form a write combined data set; and
- flushing the write combined data set to an I/O device in response to a protocol event
- according to a protocol between the I/O hub and the processor.
35. (Currently Amended) The processor medium of claim 34, wherein the plurality of partial
- writes include partial writes of a cache line, and wherein the combined write includes a full cache
- line. the protocol event includes a flushing signal from the processor, and wherein the protocol is to
- include an signaling protocol.

36. (Currently Amended) The processor medium of claim 34, wherein the external device  
includes an input/output (I/O) device to be coupled to the processor utilizing a point-to-point  
interconnect, the protocol event includes a latency condition, and wherein the protocol to include a  
timing protocol.